ABSTRACT OF THE DISCLOSURE

In a data latch timing adjustment apparatus, a read control section reads out a first checking data piece in a checking data storing section written in a memory and outputs a latch pulse signal to a delay selecting section. A selection part outputs, to a latch circuit, a delayed pulse signal obtained by delaying the latch pulse signal by the front delay circuit. The latch circuit delays the checking data piece from the memory at the reception of the delayed pulse signal. Then, the next data piece is read out from the memory and the selection part outputs, to the latch circuit, a delayed pulse signal delayed by the delay circuit at the preceding stage.